R+DDR3 PHY

Optimized for consumer applications with reduced system cost, improved performance and faster time-to-market.

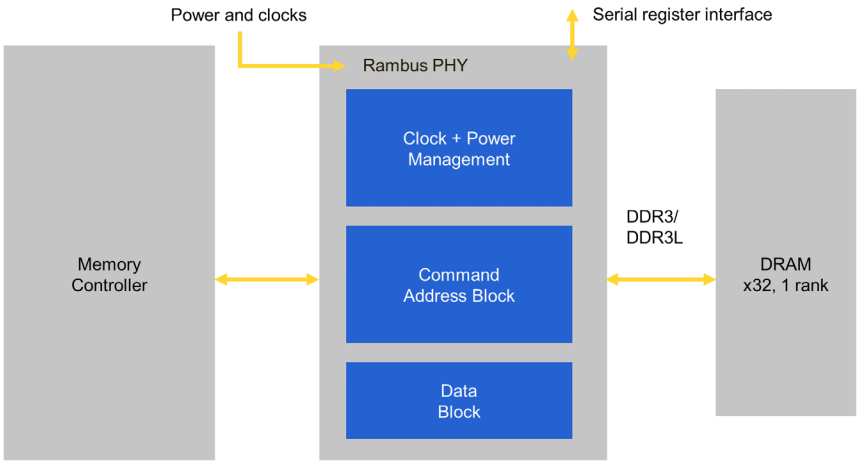
Overview

With short design windows and heightened sensitivity to costs, consumer electronics need low-risk solutions that deliver enhanced flexibility and reduced time-to-market. Designed for ease-of-integration and optimized for consumer applications, our silicon-proven R+™ DDR3 PHY delivers improved performance and margin with support for low-cost packaging and board design options. Per byte timing adjustment circuits deskew data and clock signals to improve signal integrity and simplify package and PCB system design.

Scalable up to 2133Mbps, our PHY consists of a Command/Address (C/A) macro cell and four 8-bit data macro cells. The PHY is delivered as a fully-characterized hard macro and contains all of the necessary components for robust operation including:

- IO pads
- PLL
- Power Mode Management (PMM)
- Transmit and receive paths
- Clock distribution
- Control logic
- Power distribution
- Electrostatic discharge (ESD) protection circuitry

DDR3 PHY Subsystem Example



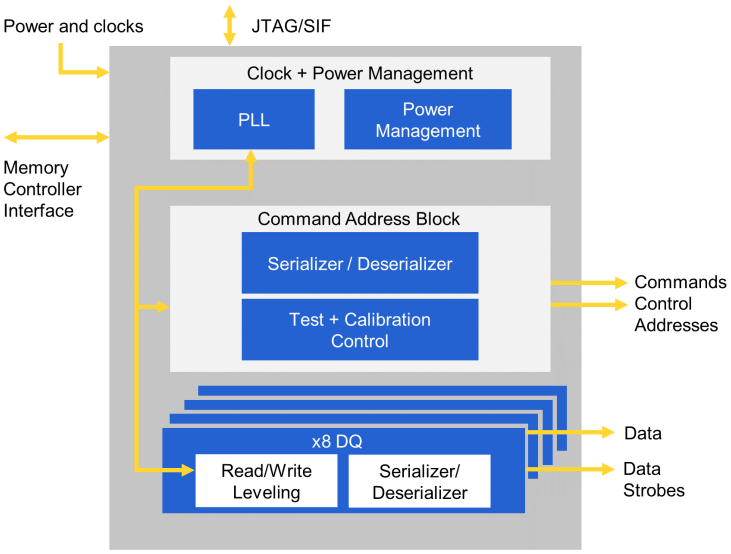
Highlights

- Available in GLOBALFOUNDRIES 28SLP process
- Compliant to JEDEC DDR3 and DDR3L
- Supports wire-bond package up to 1600Mbps; flip-chip package up to 2133Mbps
- Compatible with 4-layer and 6-layer PCBs
- DRAM on motherboard support with fly-by topology
- Includes FlexPhase™ per bit deskew of data and clock signals for simplified design
- Available option with LabStation™ Validation Platform for enhanced bring-up and validation

Standards Compatibility

Protocol	Data Rates (Mbps)
DDR3 (1.5V)	800-2133
DDR3L (1.35V)	800-1866

R+ DDR3 PHY Configuration



Features

- PLL based clocking with internal clock alignment to memory controller interface clock
- Full support for DDR3 calibration sequences such as write leveling, write training, and read training
- Single channel x32 configuration
- PHY — Controller interface gear ratio of 1:2 simplifies timing closure when integrating into SoC
- Selectable low-power operating states
- Programmable output impedance and on-die termination
- ZQ calibration of output impedance and on-die termination
- Supports wire-bond and C4 flip-chip packaging options
- Register interface for state observation enables transaction monitoring
- Test traffic generation and error checking for in-situ test
- Optional LabStation software environment for system level bring-up, characterization, and validation

Deliverables

Fully-characterized hard macro (GDSII)

Complete design views:

- Gate-level and IO models
- Verification test benches
- Layout abstracts (.lef)
- Timing models (.lib)

Full documentation:

- Datasheet
- Integration guidelines
- Package and PCB design guidelines
- ASIC/DFT manufacturing guidelines
- Test and characterization user guide
- Verilog models
- CDL netlists (.cdl)
- ATPG models
- GDSII layout
- DRC & LVS reports

Optional design integration and bring-up support services

rambus.com/ddrnphys

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